Amendments to the Specification:

Please replace paragraph **[0020]** on page 5 as follows:

The control inputs of switches 116 and 118 are connected to receive a digital input signal, which controls these switches. When the Switches 116 and 118 are closed in response to one state of the input signal, the pull-up circuit ~~104~~ 102 is activated to pull the voltage on the output node 124 high. When the switches 116 and 118 are opened in response to the other state of the input signal, the pull-up circuit 102 deactivated and the voltage on the output node 125 is pulled low by the pull-down circuit 104.

Please replace paragraph **[0030]** on page 9 as follows:

As stated above, the pull-down circuit 104 is configured in a mirror image of the pull-up circuit 102, except that complementary device types are used in the two circuits. Turning back to Fig. 1, the pull-down circuit 104 includes an output pull-down transistor 128, a reference current source 130, a feedback capacitor 134, an analog memory 136 and switches 138, 140 and 142. The pull-down transistor 128 and the switch 138 are connected in series with the output node 124 and a low voltage terminal 144, e.g., electrical ground. The drain of the pull-down transistor 128 is connected to the output node 124, while the source of the pull-down transistor is connected to the low voltage terminal 144 via the switch 138. The gate, i.e., the control terminal, of the pull-down transistor 128 is connected to the memory 136 via the switch 142. The pull-down transistor 128 is shown as an NFET. However, another type of transistor may instead be used.

Please replace paragraph **[0034]** on page 10 as follows:

The operation of the pull-down circuit 104 is now described. When the switches 138 and 140 are open during the rising edge transitions 202 and the high level sections 206, the pull-down circuit 104 is inactive. During this period, the pull-up circuit 102 is activated to pull up the voltage on the output node 124.

When the switches 138 and 140 are closed by the change in the state of the input signal at the start of the falling edge transition 204, the pull-down transistor 128 will conduct current, which tends to pull the voltage on the output node 124 low. The current conducted by the pull-down transistor 128 depends on the voltage on the gate of the transistor. Similar to the operation of the pull-up circuit 102, the initial gate voltage on the pull-down transistor 128 is provided by the memory 136. The initial gate voltage is the stored voltage from the previous operating cycle in which the pull-down transistor ~~126~~ 128 was activated. The voltage decrease on the output node 124 causes current to flow through the capacitor 134. If the falling-edge slew rate of the voltage on the output node 124 is so high that feedback current through the capacitor 134 exceeds the reference current I_{ref} provided by the current source 130, then the gate voltage of the pull-down transistor 128 will decrease. Consequently, the current flowing through the pull-down transistor 128 will decrease, which lowers the slew rate of the voltage on the output node 124.